

# SANYO Semiconductors DATA SHEET

# LA7137M — Monolithic Linear IC DVD Analog Video Output I/F IC

#### **Overview**

The LA7137M is a video output interface IC for DVD players and is optimal as the driver IC for DVD players that provide composite signal/S signal, component signal, and RGB signal video outputs.

Since this IC integrates a Y/C mixer on the same chip, the D/A converter composite output can be omitted. The LA7137M also integrates S1 and S2 DC voltage and D/A converter reference voltage generation on chip, allowing most components other than the drivers to be omitted.

#### **Functions**

- Clamps
- Amplifier
- $75\Omega$  driver
- Y/C mixer
- S1 and S2 DC output
- D/A converter reference voltage output

#### **Features**

- Video signal-to-noise ratio : -80dB
- Frequency characteristics : flat to 10MHz
- Y/C time difference : less than 2ns
- Signal dynamic range : 170IRE.
- Can support all major signal types : composite/S signals, component signals, and baseband (RGB) signals. Furthermore, the IC input type can be switched by the system microcontroller (since the input capacitors are shared).
- Two 75 $\Omega$  driver systems that can be independently muted by the system microcontroller.
- The clamp pulses required for component signal input are generated internally in the IC.
- Either of two amplifier gain levels, 8.5 and 6dB, can be selected.
- A built-in regulator circuit provides a stable DC voltage output that is independent of V<sub>CC</sub> fluctuations.

#### **Specifications**

Maximum Ratings at  $Ta = 25^{\circ}C$ 

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max		10.0	V
Allowable power dissipation	Pd max	$Ta \le 75^{\circ}C $ * Mounted on a board	525	mW
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-40 to +150	°C

\* Only when mounted on a 114.3×76.1×1.6mm<sup>3</sup> glass epoxy board

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# LA7137M

## **Operating Conditions** at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V <sub>CC</sub>		8.0	V
Operating supply voltage range	VCC op		7.6 to 8.4	V

## **Electrical Characteristics** at Ta = 25 °C, $V_{CC} = 7.6$ to 8.4 V

Parameter	Symbol	Input	Test	Conditions		Ratings		Unit
	-	signal	point		min	typ	max	
Current drain 1	ICC1			Video system current drain	14.3	17.9	21.5	mA
Current drain 2	I <sub>CC</sub> 2			75 $\Omega$ driver current drain ; no signal	14.4	18.0	21.6	mA
(A) For a pin 10 (Y signal) ir	nput when c	omposite/S	selected					
Amplifier gain (low)	G <sub>Y</sub> M	Sig.1	T13/15	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G <sub>Y</sub> H	Sig.1	T13/15	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Clamp voltage	С <sub>10</sub> Н	Sig.1	T10	The T10 sync tip potential for a 761mVp-p input	3.85	4.20	4.55	V
(B) For a pin 6 (chrominanc	e signal) inp	out when co	mposite/S	selected				
Amplifier gain (low)	G <sub>C</sub> M	Sig.2	T17/19	The gain for a 711mVp-p 3.58MHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G <sub>C</sub> H	Sig.2	T17/19	The gain for a 544mVp-p 3.58MHz signal	7.38	7.6	7.81	dB
Chrominance signal input DC voltage	D <sub>6</sub> H	Sig.2	T6	The T6 offset voltage for a 544mVp-p input	4.4	4.75	5.1	V
(C) For a pin 3 (composite s	ignal) input	when comp	posite selec	ted				
Amplifier gain (low)	G <sub>S</sub> M1	Sig.3	T21/23	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G <sub>S</sub> H1	Sig.3	T21/23	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Clamp voltage	С <sub>3</sub> н	Sig.3	T3	The T3 sync tip potential for a 761mVp-p input	4.0	4.35	4.7	V
(D) For a pins 6 and 10 (S s	ignal) input	when S is s	selected					
Amplifier gain (low)	G <sub>S</sub> M2	Sig.1 Sig.2	T21/23	The gain for a 996mVp-p 100kHz signal or a 711mVpp 3.58kHz signal	4.92	5.27	5.61	dB
Amplifier gain (high)	G <sub>S</sub> H2	Sig.1 Sig.2	T21/23	The gain for a 761mVp-p 100kHz signal or a 544mVpp 3.58kHz signal	7.25	7.6	7.94	dB
(E) The gain ratios between	the differer	nt signals w	hen compos	site is selected				
Y/chrominance amplifier gain ratio	ΔYC	Sig.1 Sig.2	T13/15 T17/19	The ratio of the $G_YH$ gain for (A) and the $G_CH$ gain for (B)	-3	0	3	%
Y/composite amplifier gain ratio	∆Y <sub>S</sub> 1	Sig.1 Sig.3	T13/15 T21/23	The ratio of the $G_YH$ gain for (A) and the $G_SH1$ gain for (C)	-3	0	3	%
Chrominance/composite amplifier gain ratio	∆C <sub>S</sub> 1	Sig.2 Sig.3	T17/19 T21/23	The ratio of the $G_CH$ gain for (B) and the $G_SH1$ gain for (C)	-3	0	3	%
(F) The gain ratios between	the differer	nt signals wi	hen S is sel	ected				
Y/S amplifier gain ratio	∆Y <sub>S</sub> 2	Sig.1 Sig.2	T13/15 T21/23	The ratio of the $G_YH$ gain for (A) and the $G_SH2$ gain for (D)	-4.5	0	4.5	%
Chrominance/S amplifier gain ratio	∆C <sub>S</sub> 2	Sig.1 Sig.2	T17/19 T21/23	The ratio of the $G_CH$ gain for (B) and the $G_SH2$ gain for (D)	-4.5	0	4.5	%
(G) The pin 10 (Y signal) inp	out when co	mponent is	selected					
Amplifier gain (low)	G <sub>Y</sub> M	Sig.1	T13/15	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G <sub>Y</sub> H	Sig.1	T13/15	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Y input clamp voltage	с <sub>10</sub> н	Sig.1	T10	The T10 sync tip potential for a 761mVp-p input	3.85	4.20	4.55	V
(H) The pin 6 (B-Y or R-Y si	gnal) input	when comp	onent is sel	ected				
Amplifier gain (low)	G <sub>N</sub> M	Sig.4	T17/19	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G <sub>N</sub> H	Sig.4	T17/19	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Input pedestal clamp voltage	P <sub>6</sub> H	Sig.4	T6	The T6 pedestal potential for a 761 mVp-p input	4.4	4.75	5.1	V

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Parameter	Symbol	Input	Test	Conditions		Ratings		Unit
1 didineter	Cymbol	signal	point	Conditions	min	typ	max	Ollin
(I) The pin 3 (B-Y or R-Y sig	nal) input w	hen compo	onent is sele	cted				
Amplifier gain (high)	G <sub>N</sub> H	Sig.4	T21/23	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Input pedestal clamp voltage	P <sub>3</sub> H	Sig.4	Т3	The T3 pedestal potential for a 761 mVp-p input	4.4	4.75	5.1	V
(J) The gain ratios between	the differen	t signals wi	nen compor	ent is selected		1		
Y/component amplifier gain ratio 1	ΔΥ1	Sig.1 Sig.4	T13/15 T17/19	The ratio of the $G_YH$ gain for (E) and the $G_NH$ gain for (F)	-3	0	3	%
Y/component amplifier gain ratio 2	ΔΥ2	Sig.1 Sig.4	T13/15 T21/23	The ratio of the $G_YH$ gain for (E) and the $G_NH$ gain for (G)	-3	0	3	%
Component amplifier gain ratio	ΔΝ	Sig.4 Sig.4	T17/19 T21/23	The ratio of the $G_NH$ gain for (F) and the $G_NH$ gain for (G)	-3	0	3	%
(K) The pin 10 (RGB signal)	) input when	5						
Amplifier gain (low)	G <sub>B</sub> M	Sig.1	T13/15	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G <sub>B</sub> H	Sig.1	T13/15	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Input clamp voltage	с <sub>10</sub> н	Sig.1	T10	The T10 sync tip potential for a 761mVp-p input	3.85	4.20	4.55	V
(L) The pin 6 (RGB signal) i	nnut when b	l Jaseband is	selected	1.77				
Amplifier gain (low)	r.	1	T13/15	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
,	G <sub>B</sub> M	Sig.1	T13/15		5.05 7.38	5.27	5.48 7.81	dB
Amplifier gain (high) Input clamp voltage	G <sub>B</sub> H C <sub>6</sub> H	Sig.1 Sig.1	T10/15	The gain for a 761mVp-p 100kHz signal The T10 sync tip potential for a 761mVp-p	4.0	4.35	4.7	V
				input				
(M) The pin 3 (RGB signal)	input when	baseband i	s selected					
Amplifier gain (low)	G <sub>B</sub> M	Sig.1	T13/15	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G <sub>B</sub> H	Sig.1	T13/15	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Input clamp voltage	С <sub>3</sub> Н	Sig.1	T10	The T10 sync tip potential for a 761mVp-p input	4.0	4.35	4.7	V
(N) The gain ratios between	the differen	nt signals w	hen baseba	ind is selected				
Baseband amplifier gain	ΔB1	Sig.1	T13/15	The ratio of the $G_BH$ gain for (I) and the	-3	0	3	%
ratio 1		Sig.1	T17/19	G <sub>B</sub> H gain for (J)				
Baseband amplifier gain ratio 2	Δ <b>B</b> 2	Sig.1 Sig.1	T13/15 T21/23	The ratio of the $G_{B}H$ gain for (I) and the $G_{B}H$ gain for (K)	-3	0	3	%
Baseband amplifier gain	Δ <b>B</b> 3	Sig.1	T17/19	The ratio of the G <sub>B</sub> H gain for (J) and the	-3	0	3	%
ratio 3		Sig.1	T21/23	G <sub>B</sub> H gain for (K)				
(O) Gain frequency character	eristics (Cor	mmon to all	modes and	input signals other than Y/C mixed mode)				
6MHz low-pass filter attenuation	F <sub>Y</sub> 6	Sig.1	T13/15	The difference between $G_YH$ and the gain for a 761mVp-p, 6MHz input	-0.5	0	+0.5	dB
10MHz low-pass filter attenuation	F <sub>Y</sub> 10	Sig.1	T13/15	The difference between G <sub>Y</sub> H and the gain for a 761mVp-p, 10MHz input	-0.5	0	+0.5	dB
(P) DC voltage when output	muting apr	l blied (Comn	non to all me	odes)				
Pin 13 voltage	V <sub>13</sub>		T13	· · · · · · · · · · · · · · · · · · ·	3.7	4.05	4.4	V
Pin 15 voltage	V <sub>15</sub>		T15		3.7	4.05	4.4	V
Pin 17 voltage	V <sub>17</sub>		T17		3.9	4.25	4.6	V
Pin 19 voltage	V <sub>19</sub>		T19		3.9	4.25	4.6	V
Pin 21 voltage	V <sub>21</sub>		T21		3.9	4.25	4.6	V
Pin 23 voltage	V <sub>23</sub>		T23		3.9	4.25	4.6	V
(Q) Output DC voltage char		1	1			I		
D/A converter reference voltage	V <sub>DA</sub>		T12	When driving an 800µA load current	3.2	3.4	3.6	V
4 : 3 output mode DC	V <sub>43</sub>		T16	In 4 : 3 control mode (no load)	0	0.01	0.35	V
Letterbox output DC	V <sub>LB</sub>		T16	In letterbox control mode (when driving a 500μA load current)	2.05	2.2	2.35	V
Squeezed output DC	V <sub>SQ</sub>		T16	In squeeze control mode (when driving a 500µA load current)	4.4	4.7	5.0	V

Note : The amplifier gain and amplifier gain ratios are the values when the components shown in the test circuit diagram are all connected.

## LA7137M

Cumbel.			Control volt	age (unit: V)			Switching conditions			
Symbol	VDC1	VDC2	VDC4	VDC5	VDC11	VDC22	SW1	SW2		
I <sub>CC</sub> 1	0	0	3.3	0	3.3	3.3	ON	ON		
I <sub>CC<sup>2</sup></sub>	0	0	3.3	0	3.3	3.3	ON	ON		
A) For a pin 10 (Y sig	nal) input when o	composite/S sel	ected							
G <sub>Y</sub> M	0/3.3	0	-	-	0	3.3	ON/OFF	ON		
G <sub>Ү</sub> Н	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON		
С <sub>10</sub> Н	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON		
(B) For a pin 6 (chrom	ninance signal) in	put when comp	osite/S selected	d						
G <sub>C</sub> M	0/3.3	0	-	-	0	3.3	ON/OFF	ON		
G <sub>C</sub> H	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON		
С <sub>6</sub> н	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON		
(C) For a pin 3 (comp	osite signal) inpu	t when composi	te selected							
G <sub>S</sub> M1	0/3.3	0	-	-	0	3.3	ON/OFF	ON		
G <sub>S</sub> H1	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON		
С <sub>3</sub> н	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON		
(D) For a pins 3 (S sig	nal) input when	S is selected								
G <sub>S</sub> M2	0/3.3	0	-	-	0	3.3	ON/OFF	ON		
G <sub>S</sub> H2	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON		
(E) The gain ratios be	tween the differe	nt signals when	composite is s	elected		11				
ΔYC	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON		
ΔY <sub>S</sub> 1	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON		
∆C <sub>S</sub> 1	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON		
(F) The gain ratios be	tween the differe	nt signals when	S is selected			11				
ΔY <sub>S</sub> 2	0/3.3	0	-	-	3.3	0	ON/OFF	ON		
∆C <sub>S</sub> 2	0/3.3	0	-	-	3.3	0	ON/OFF	ON		
(G) The pin 10 (Y sigr	nal) input when c	omponent is sel	ected			11				
GYM	0/3.3	3.3	-	-	0	3.3	ON/OFF	ON		
G <sub>Y</sub> H	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON		
С <sub>10</sub> Н	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON		
(H) The pin 6 (B-Y or	R-Y signal) input	when compone	nt is selected			11				
G <sub>N</sub> M	0/3.3	3.3	-	-	0	3.3	ON/OFF	ON		
G <sub>N</sub> Н	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON		
P <sub>6</sub> H	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON		
(I) The pin 3 (B-Y or F	R-Y signal) input v	when componer	nt is selected			1	I			
G <sub>N</sub> M	0/3.3	3.3	-	-	0	3.3	ON/OFF	ON		
G <sub>N</sub> H	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON		
P <sub>3</sub> H	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON		
(J) The gain ratios be	tween the differen	nt signals when	component is s	selected		<u> </u>	I			
ΔΥ1	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON		
ΔΥ2	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON		
ΔN	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON		
(K) The pin 10 (RGB :	signal) input whe	n baseband is s	elected	1	1	1 1				
G <sub>B</sub> M	0/3.3	-	-	-	0	3.3	ON/OFF	OFF		
G <sub>B</sub> H	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF		
С <sub>10</sub> Н	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF		
(L) The pin 6 (RGB si				1						
G <sub>B</sub> M	0/3.3	-	-	-	0	3.3	ON/OFF	OFF		
G <sub>B</sub> H	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF		
C <sub>6</sub> H	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF		
(M) The pin 3 (RGB s				I						
G <sub>B</sub> M	0/3.3	-	-	-	0	3.3	ON/OFF	OFF		
GBH	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF		
~ <u>D</u> , ,	0,0.0				0.0	0.0	0.1/011	0.1		

### Switching Characteristics ("-" indicates OK under all conditions)

0			Control volt	age (unit: V)			Switching	Switching conditions	
Symbol	VDC1	VDC2	VDC4	VDC5	VDC11	VDC22	SW1	SW2	
N) The gain ratios b	between the differe	ent signals whe	n baseband is s	elected					
Δ <b>B</b> 1	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF	
∆B2	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF	
∆B3	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF	
O) Gain frequency	characteristics (Co	ommon to all me	odes and input	signals other the	an Y/C mixed m	node)			
F <sub>Y</sub> 6	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON	
F <sub>Y</sub> 10	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON	
P) DC voltage when	n output muting ap	plied (Commor	to all modes)						
V <sub>13</sub>	0	-	-	-	0/3.3	0/3.3	ON	-	
V <sub>15</sub>	3.3	-	-	-	0/3.3	0/3.3	ON	-	
V <sub>17</sub>	0	-	-	-	0/3.3	0/3.3	ON	-	
V <sub>19</sub>	3.3	-	-	-	0/3.3	0/3.3	ON	-	
V <sub>21</sub>	0	-	-	-	0/3.3	0/3.3	ON	-	
V <sub>23</sub>	3.3	-	-	-	0/3.3	0/3.3	ON	-	
Q) Output DC volta	ge characteristics								
V <sub>DA</sub>	-	-	-	-	0/3.3	0/3.3	-	-	
V <sub>43</sub>	-	-	0	0	0/3.3	0/3.3	-	-	
V <sub>LB</sub>	-	-	0	3.3	0/3.3	0/3.3	-	-	
V <sub>SQ</sub>	-	-	3.3	0	0/3.3	0/3.3	-	-	

#### **Control Pin Functions**

Pin No.	Pin state	Low	Ор	en	High		
1	Pin voltage	0 to 0.6V	1.55 to	1.75V	2.7 to 5V		
	$75\Omega$ driver muting	13, 17, 21 muted	Not muted		15, 19, 23 muted		
2	Pin voltage	0 to 0.6V	1.55 to 1.75V		2.7 to 5V		
	Signal input type switching	Signal input type switching Composite/S mode Baseband mode					
11	Pin voltage	0 to 1V		2.7 to 8V (note)			
	Amplifier gain switching	6dB			8.5dB		
22	Pin voltage	0 to 1V	0 to 1V		2.7 to 8V (note)		
	Y/C mixer control	Y/C mixed mode			Composite mode		

Note : Never apply a voltage higher than the V<sub>CC</sub> voltage at pins 9 and 20 to pin 11 or pin 22.

\* : Y/C mixed mode is illegal in modes other than composite/S mode.

\* : In composite mode, use pin 6 to input the chrominance signal capacitor-coupled, pin 3 for the clamped composite signal, and pin 10 for the clamped Y signal. However, in S mode, pin 3 will have no input.

In component mode, pins 3 and 6 will be pedestal clamped B-Y and R-Y signals, respectively, while pin 10 will be the clamped Y signal input.

In baseband mode, pins 3, 6, and 10 are all clamped inputs, for the RGB signals, respectively. Pins 11 and 22 must never be left open.

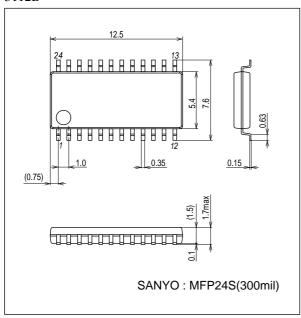
Pin 4	Pin 5	Pin 16 output DC		
0 to 1V	0 to 1V	Low (0V) $\rightarrow$ 4 : 3 mode		
0 to 1V	2.6 to 5V	Middle (2.5V) $\rightarrow$ Letterbox mode		
2.6 to 5V	0 to 1V	High (5V) $\rightarrow$ Squeezed mode		
2.6 to 5V	2.6 to 5V	Illegal values		

#### **Design Guaranteed Items** (at $Ta = 25^{\circ}C$ )

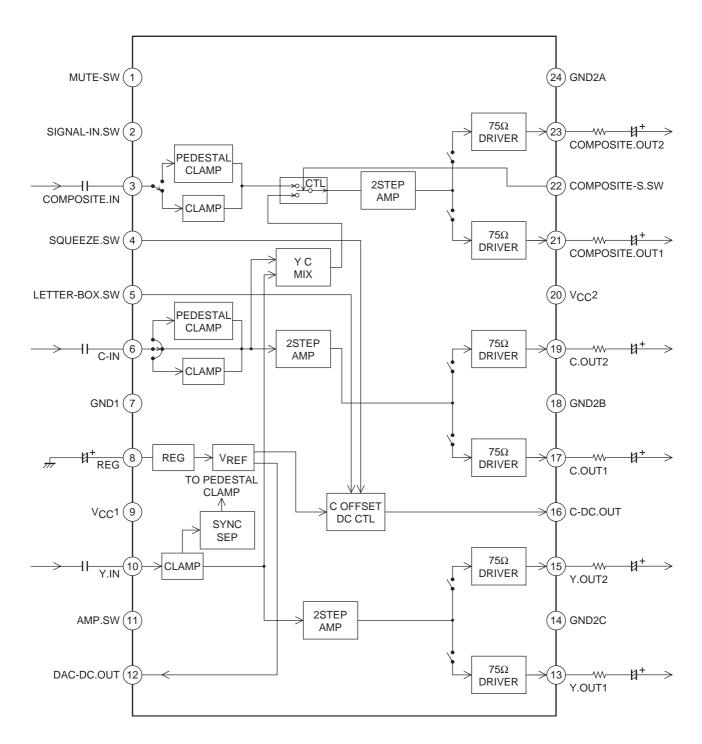
Parameter	Symbol	Conditions		Ratings		Unit
Farameter	Symbol	Conditions	min	typ	max	Unit
<modes c="" mix<="" other="" td="" than="" y=""><td>ed Mode&gt;</td><td></td><td></td><td></td><td></td><td></td></modes>	ed Mode>					
Inter-channel crosstalk	СТ	Input an f = 4MHz signal to another channel such that the		-65	-60	dB
		capacitor-coupled output becomes 1Vp-p. Measure the				
		amplitude of the 4MHz component on the monitored channel.				
		This parameter is stipulated to be the ratio of that level with the				
		amplitude of the 4MHz component on that other channel.				
Video signal-to-noise ratio	SN	Input a white 100% signal and apply a 3.3V level to pin 11.		-80	-78	dB
		Measure the signal-to-noise ratio in the output signal.				
Differential gain	DG	Input a standard 1Vp-p staircase signal (color) and leave pin 11		0.5	2	%
		open. Measure the differential gain in the output signal. Note				
		that the components shown in the test circuit diagram for this				
		parameter must be inserted at this time.				
Differential phase	DP	Input a standard 1Vp-p staircase signal (color) and leave pin 11	-1	0	1	dB
		open. Measure the differential phase in the output signal. Note				
		that the components shown in the test circuit diagram for this				
		parameter must be inserted at this time.				
<y c="" mixed="" mode=""></y>						
Inter-channel crosstalk	СТ	Input an f = 4MHz signal to another channel such that the		-65	-60	dB
		capacitor-coupled output becomes 1Vp-p. Measure the				
		amplitude of the 4MHz component on the monitored channel.				
		This parameter is stipulated to be the ratio of that level with the				
		amplitude of the 4MHz component on that other channel.				
Video signal-to-noise ratio	SN	Input a white 100% signal and apply a 3.3V level to pin 11.		-74	-72	dB
		Measure the signal-to-noise ratio in the output signal.				
Differential gain	DG	Input a standard 761mVp-p staircase signal (color) and apply a		4	5.5	%
		3.3V level to pin 11. Measure the differential gain in the output				
		signal. Note that the components shown in the test circuit				
		diagram for this parameter must be inserted at this time.				
Differential phase	DP	Input a standard 761mVp-p staircase signal (color) and apply a	-1	0.5	1.5	dB
		3.3V level to pin 11. Measure the differential gain in the output				
		signal. Note that the components shown in the test circuit				
		diagram for this parameter must be inserted at this time.				

# Package Dimensions

unit : mm (typ) 3112B



#### **Block Diagram**



## **Pin Functions**

For more information on the pin functions, see the I/O circuit diagrams, and for an operating description, see the block diagram.

Note that the data shown below consists of typical values and that detailed ratings are provided in the Electrical Characteristics.

	acteristics.	<b>-</b>	r	1		1
Pin No.	Pin	I/O	Pin voltage	I/O impedance	Description	Equivalent circuit
10	Y-IN	1	4.2V	Clamp form	Input pin for either the Y or a baseband signal. This pin is used for the Y signal for composite/S and component signal input, and for one of the RGB signals with sync. Keyed clamping (clamping at the lowest point in the signal, that is, at the sync tip) is applied whichever signal is input. If a component signal is input, sync separation is performed and a clamp pulse for pedestal clamping is produced. The clamped signal is amplified by an amplifier that can be switched between two levels so that it becomes 2/p-p with an output amplitude of 140IRE.	
13	Y.OUT1	0	2.7V	11.6Ω	75Ω driver output for the signal input to pin 10. The pin 10 output signal is split into two, and one is passed through a muting circuit that mutes when pin 1 is low (0V) and output to the 75Ω driver.	VCC CG VCC VCC OUT CO OUT
15	Y.OUT2	0	2.7V	11.6Ω	$75\Omega$ driver output for the signal input to pin 10. Of the pin 10 input signals, the other signal is passed through a muting circuit that mutes when pin 1 is high (3.3 to 5.0V) and output to the $75\Omega$ driver.	VCC VCC VCC VCC VCC VCC VCC VCC
6	C-IN	1	4.8V	10kΩ	Input pin for chrominance, component, and baseband signals. The chrominance signal must be input to this pin when a composite/S signal input is used. The signal must be capacitor coupled. The B-Y or R-Y signal must be input to this pin when a component signal is input. The signal is clamped at the pedestal level. Any one of the RGB with sync signals must be input to this pin when a baseband signal is input. Keyed clamping will be applied to the signal. The capacitor coupled or clamped signal is amplified by an amplifier that can be switched between two levels so that it becomes 2Vp-p with an output amplitude of 140IRE.	VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC

Continu	and from preceding page.					
Pin	Pin	I/O	Pin	I/O	Description	Equivalent circuit
No. 17	C.OUT1	0	voltage 3.9V	impedance 11.6kΩ	75Ω driver output for the signal input to pin 6. The pin 6 output signal is split into two, and one is passed through a muting circuit that mutes when pin 1 is low (0V) and output to the 75Ω driver.	VCC VCC VCC VCC VCC VCC VCC VCC
19	C.OUT2	0	3.9V	11.6kΩ	75Ω driver output for the signal input to pin 6. Of the pin 10 input signals, the other signal is passed through a muting circuit that mutes when pin 1 is high (3.3 to 5.0V) and output to the 75Ω driver.	VCC CC VCC VCC VCC VCC VCC VCC
3	COMPOSITE.IN	I	4.5V	Clamp form	Input pin for composite, component, and baseband signals. If a composite signal is input, it must be input to this pin, and if a baseband signal is input, any one of the RGB with sync signals must be input to this pin. Keyed clamping will be applied to the signal. For S signal input, this pin must be dropped to ground. For component signal input, input either the B-Y or R-Y signal to this pin. The signal will be clamped at the pedestal level. The clamped signal is amplified by an amplifier that can be switched between two levels so that it becomes 2Vp-p with an output amplitude of 140IRE.	VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC
21	COMPOSITE. OUT1	0	3.57V	11.6Ω	75Ω driver output for the signal input to pin 3. The pin 3 output signal is split into two, and one is passed through a muting circuit that mutes when pin 1 is low (0V) and output to the 75Ω driver.	VCC GG VCC VCC VCC VCC VCC VCC

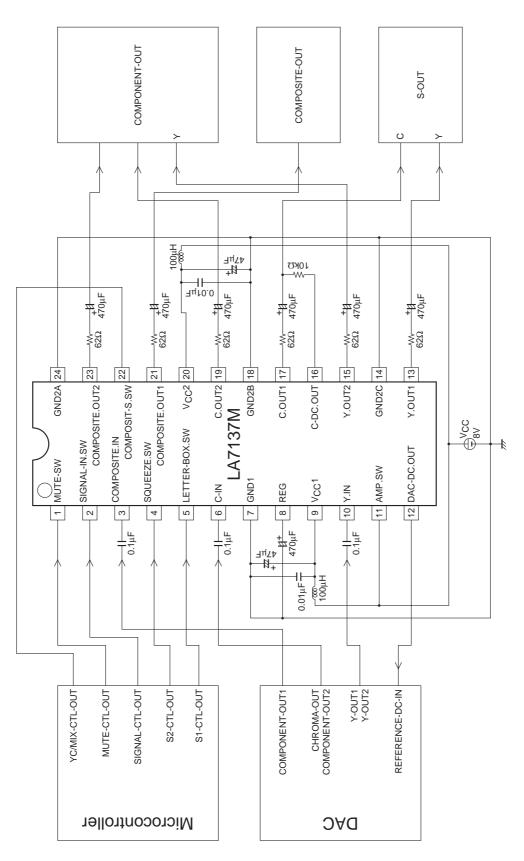
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Pin No.	Pin	I/O	Pin voltage	I/O impedance	Description	Equivalent circuit
23	COMPOSITE. OUT2	0	3.57V	11.6Ω	$75\Omega$ driver output for the signal input to pin 3. Of the pin 3 input signals, the other signal is passed through a muting circuit that mutes when pin 1 is high (3.3 to 5.0V) and output to the $75\Omega$ driver.	
1	MUTE-SW	I	1.7V	21kΩ	Controls the muting applied to the output signals. This pin can be controlled from a 3.3 to 5V power supply microcontroller. (See the control pin function table.)	4.25V VCC
2	SIGNAL-IN.SW	1	1.7V	21kΩ	Switches the input circuit types of pins 3 and 6 to match the type of the input signal. This pin can be controlled from a 3.3 to 5V power supply microcontroller. (See the control pin function table.)	4.25V VCC $\downarrow$
4	SQUEEZE.SW	I	2.40V	9.0GΩ	Inputs squeeze control information from the system microcontroller. This pin can be controlled from a 3.3 to 5V power supply microcontroller. (See the control pin function table.)	Vcc N o 5kΩ m m m
5	LETTER-BOX.SW	I	2.43V	8.1GΩ	Inputs letterbox control information from the system microcontroller. This pin can be controlled from a 3.3 to 5V power supply microcontroller. (See the control pin function table.)	Vcc

Continu	ed from preceding page.					
Pin No.	Pin	I/O	Pin voltage	I/O impedance	Description	Equivalent circuit
16	C-DC.OUT	0	4.7V	4.1Ω	The LA7137M creates, and outputs from this pin, a stabilized DC voltage based on the control information input to pins 4 and 5. This pin outputs a low level (0V) for 4 : 3 mode, a middle level (2.2V) for letterbox mode, and a high level (5V) for squeeze mode. A $10k\Omega$ resistor must be inserted to superimpose the DC voltage output from pin 17 on the capacitor coupled chrominance output. (See the application circuit diagram.)	
11	AMP-SW	I	2.4V	9.0GΩ	Control pin that switches the amplifier gain to match the amplitude of the input signal. This pin's input level can be switched between $V_{CC}$ and ground on the printed circuit board even by a 3.3 to 5.0V power supply microcontroller. (See the control pin functions table.)	
22	COMPOSITE- S.SW	Ρ	2.4V	9.0GΩ	Controls the on/off state of the Y/C mixer. When using a D/A converter that omits the composite output, the Y/C mixer must be turned on. At the same time as mixing the Y signal input to pin 10 with the chrominance signal input to pin 6, pin 3 will be dropped to ground. When pin 2 control specifies a signal type other than composite/S signal, this pin must be tied high. This pin's input level can be switched between $V_{CC}$ and ground on the printed circuit board even by a 3.3 to 5.0V power supply microcontroller. (See the control pin functions table.)	Vcc Vcc Vcc Vcc Vcc Vcc Vcc Vcc
12	DAC-DC.OUT	0	3.4V	4.0Ω	Outputs a DC reference voltage for use by a D/A converter. In particular, it outputs a 3.3V level. This reference voltage is unaffected by $V_{CC}$ fluctuations or temperature and can be used in conjunction with a resistor divider to produce the DC level required by the D/A converter.	
7	GND1	Ρ	0V		Ground for systems other than the $75\Omega$ driver system.	

Continu	ed from preceding page.					
Pin No.	Pin	I/O	Pin voltage	I/O impedance	Description	Equivalent circuit
8	REG	0	4.35V	1.5kΩ	External pin for the regulator circuit that creates the IC internal reference voltage. Since the IC internal noise is influenced by the stability of this regulator, we recommend connecting a $470\mu$ F capacitor to this pin to if assuring a -80dB signal-to-noise ratio is required.	12k0 29.2k0 12k0 29.2k0 10pF 10pF 10pF 10pF
9	V <sub>CC</sub> 1	Ρ	8V		$V_{CC}$ (8V applied) for systems other than the 75 $\Omega$ driver system. Insert a 47 $\mu$ F capacitor between this pin and pin 7.	
20	V <sub>CC</sub> 2	Ρ	8V		$V_{CC}$ (8V applied) for the 75 $\Omega$ driver system. Insert a 47 $\mu$ F capacitor between this pin and pin 14, 18, or 24. The PCB layout related to this pin requires care due to the large amplitude output signals handled.	
14	GND2C	Р	0V		Ground for the 75Ω driver system (pin 13 or 15). The PCB layout related to this pin requires care due to the large amplitude output signals handled.	
18	GND2B	Р	0V		Ground for the $75\Omega$ driver system (pin 17 or 19). The PCB layout related to this pin requires care due to the large amplitude output signals handled.	
24	GND2A	Ρ	0V		Ground for the $75\Omega$ driver system (pin 21 or 23). The PCB layout related to this pin requires care due to the large amplitude output signals handled.	

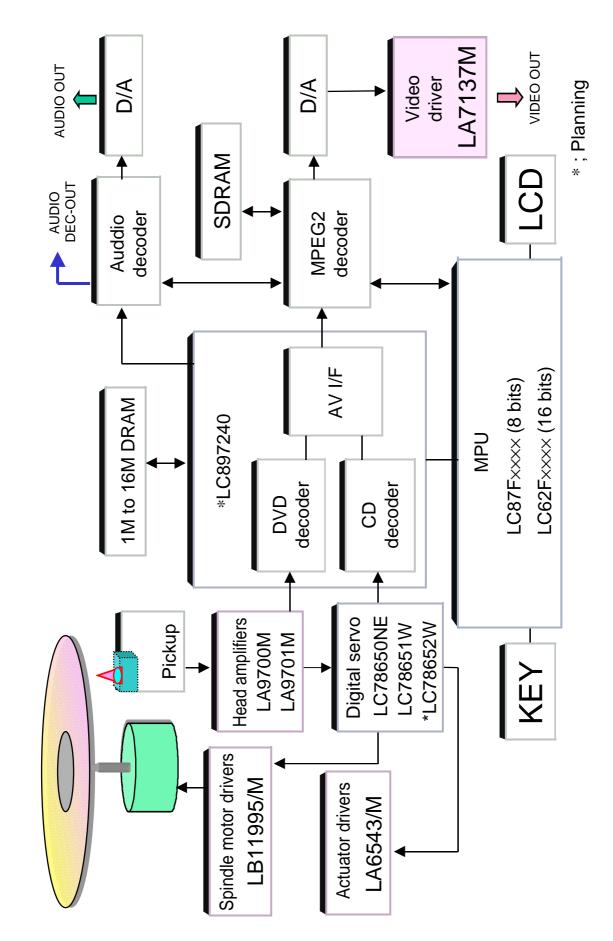
## **Sample Application Circuit**

Single composite/S signal plus single component signal application using a single D/A converter



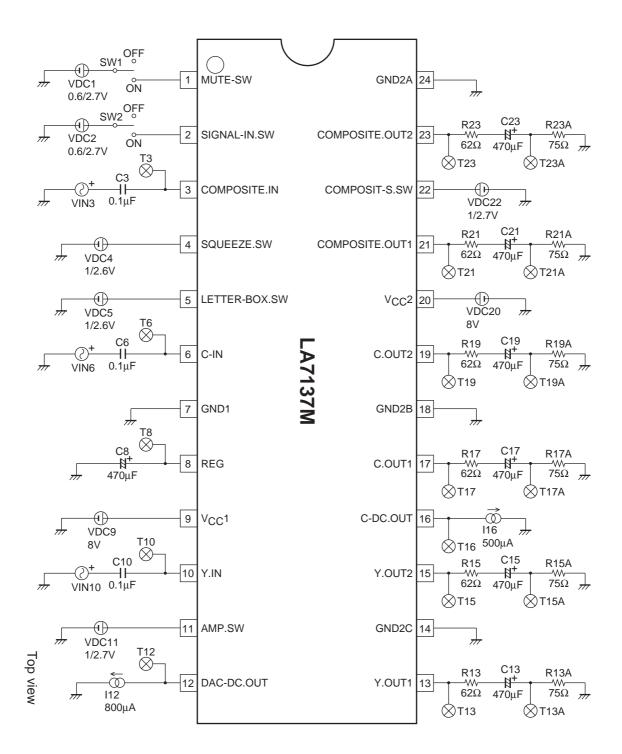
Application circuit diagram for end product that provides one output system each for composite/S and component outputs and the D/A converter output pin is shared between the S signal and the component signal systems. The muting control can be used to switch between the composite/S and component outputs.

The system microcontroller must be programmed to turn the Y/C mixer off when the component signal system is used.

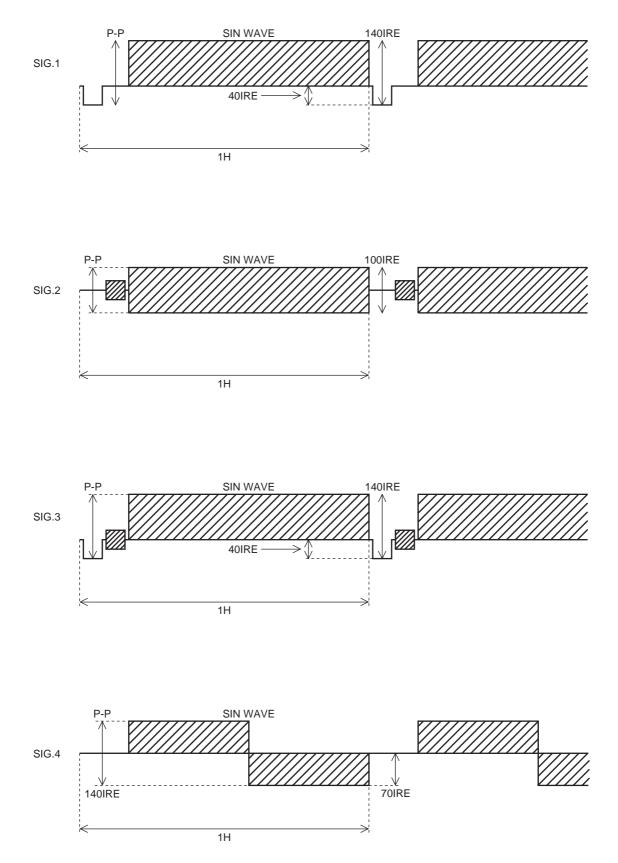


## **DVD Video Player System Block Diagram**

## **Test Circuit**



# Input Signal for Test



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